**February 2nd Senior Project Meeting**

**Armstrong Hall 148: 2:00PM –**

**Members in Attendance:** All Members

* Zachary
  + Last Week
    - Created the presentation
    - Worked on the I2S/Filter Subsystem
    - Updated the top-level drawing
    - Created an updated schedule
    - Added all code to chip.v
      * All Verilog code is in chip.v and is synthesizable
      * Need help with a testbench